**Scholar** **All articles** Recent articles Results **1** - **10** of about **59,200**. (**0.17** sec)

**Speculative** execution via **address** prediction and data prefetching- ▶psu.edu [PDF]
J González, A González - Proceedings of the 11th international conference on ..., 1997 - portal.acm.org
**...** load/ **store** using their last effective **address** and a **...** Predicted loads and **stores** are issued speculatively **...** **Instructions** that depend on **speculative** loads are also **...**
Cited by 120 - Related articles - All 18 versions

**Speculative** versioning cache- ▶kfupm.edu.sa [PDF]
S Gopal, TN Vijaykumar, JE Smith, GS Sohi - Proceedings of the 4th International Symposium on ..., 1998 - doi.ieeecomputersociety.org
**...** Mul- tiple **speculative stores** to the same location create multiple versions **...** If a load is to the same **address** as a **...** can use data bypassed from the **store** when the **...**
Cited by 222 - Related articles - All 37 versions

**Speculative** precomputation: long-range prefetching of delinquentloads- ▶licm.fr [PDF]
JD Collins, H Wang, DM Tullsen, C Hughes, ... - ... Proceedings. 28th Annual International Symposium on, 2001 - ieeexplore.ieee.org
**...** the thread context with the **address** of the **... Speculative** threads must not update the architectural state, for example, by exe- cuting a **store instruction**. **...**
Cited by 233 - Related articles - BL Direct - All 20 versions

**Speculative** lock elision: Enabling highly concurrent multithreaded execution- ▶kfupm.edu.sa [PDF]
R Rajwar, JR Goodman - Proceedings of the 34th annual ACM/IEEE ..., 2001 - portal.acm.org
**...** commit **speculative** state, and exit **speculative** critical section **...** is elided speculatively, and a future **store** matching the **...** load (ldl_l) to an **address** is followed **...**
Cited by 202 - Related articles - BL Direct - All 30 versions

Clustered **speculative** multithreaded processors- ▶psu.edu [PDF]
P Marcuello, A González - Proceedings of the 13th international conference on ..., 1999 - portal.acm.org
**...** When a new thread is spawned, the effective **address** of each **store instruction** is predicted as the **...** type of trace, the control flow of **speculative** loop traces **...**
Cited by 206 - Related articles - All 44 versions

Using **speculative** retirement and larger **instruction** windows to narrow the performance ...- ▶psu.edu [PDF]
P Ranganathan, VS Pai, SV Adve - Proceedings of the ninth annual ACM symposium on ..., 1997 - portal.acm.org
**...** potentially increase the overlap available to **stores** and **address** the **store** latency responsible **...** PC and SC, the two techniques of **speculative** retirement and **...**
Cited by 69 - Related articles - All 11 versions

[PDF] ▶Memory **address** prediction for data speculation
J González, A González - Lecture notes in computer science, 1997 - Citeseer
**...** This paper shows that load/**store instructions** are very good candidates for **speculative** execution since their eective **address** is highly predictable. **...**
Cited by 37 - Related articles - View as HTML - BL Direct - All 15 versions

The **store**-load **address** table and **speculative** register promotion- ▶ kfupm.edu.sa [PDF]
M Postiff, D Greene, T Mudge - Proceedings of the 33rd annual ACM/IEEE ..., 2000 - portal.acm.org
**...** To initialize a **speculative** promotion, a spe- cial map **...** the data at the given memory **address** resides in **...** are essentially just special load and **store** operations. **...**
Cited by 29 - Related articles - BL Direct - All 12 versions

Zero-cycle loads: Microarchitecture support for reducing load latency- ▶ ucdavis.edu [PS]
TM Austin, GS Sohi - Proceedings of the 28th annual international ..., 1995 - portal.acm.org
**...** An interlock through memory occurs whenever an earlier **store instruction** with a **...** If fast **address** calculation fails, a non-**speculative** effective **address** can be **...**
Cited by 98 - Related articles - BL Direct - All 5 versions

A comprehensive **instruction** fetch mechanism for a processor supporting **speculative** ...- ▶ kfupm.edu.sa [PDF]
TY Yeh, YN Patt - ACM SIGMICRO Newsletter, 1992 - portal.acm.org
**...** for a superscalar processor sup- porting **speculative** execution. **...** buffer for the return **instruction** to **store** branch- type **...** the top of the return **address** stack is **...**
Cited by 87 - Related articles - BL Direct - All 11 versions

Gooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next